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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Paper No. 24

Serial Number: 08/193,634
Filing Date: February 8, 1994
Appellant(s): James E. Trounson

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BOARD OF PATENT APPEALS
AND INTERFERENCES

95-2784
James A. LaBarre
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal
filed 11-21-94.

(1) *Status of claims.*

The statement of the status of claims contained in the brief
is correct.

(2) *Status of Amendments After Final.*

The appellant's statement of the status of amendments after
final rejection contained in the brief is correct.

(3) *Summary of invention.*

The summary of invention contained in the brief is correct.

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(4) *Issues.*

The appellant's statement of the issues in the brief is correct.

(5) *Grouping of claims.*

Appellant's brief includes a statement that claims 1-3 and 18-19 do not stand or fall together and provides reasons as set forth in 37 C.F.R. § 1.192(c)(5) and (c)(6).

(6) *Claims appealed.*

The copy of the appealed claims contained in the Appendix to the brief is correct.

(7) *Prior Art of record.*

The following is a listing of the prior art of record relied upon in the rejection of claims under appeal.

4,829,419 Hyatt 5-1989

4,786,847 Daggett et al. 11-88

(9) *Grounds of rejection.*

The following ground(s) of rejection are applicable to the appealed claims.

Please refer to the final action mailed 4-21-94.

(10) *New ground of rejection.*

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This Examiner's Answer does not contain any new ground of rejection.

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(11) *Response to argument.*

With respect to claim 1, applicant argues that Hyatt discloses active processors in figure 3, in addition to the active processor 12 disclosed in figure 1; thus Hyatt fails to meet the single processor limitation set forth in claim 1. However, in order for any of the digital circuit components disclosed in figure 3 to be processors they must comprise a CPU. Clearly, these elements of figure 3 are not processors since none of them have a CPU.

Applicant attempts to buttress his argument discussed above by referring to a definition of "active" set forth in the specification. He contends that the circuitry disclosed by Hyatt in figure 3 falls within his "active" definition thereby constituting an active processor. However, as discussed above, an electronic device can only be defined as a processor if it comprises a CPU, and as stated previously none of the elements in figure 3 comprise a CPU.

Further, with respect to claim 1, Hyatt discloses a single processor 12 for translating defined data into servo commands and receiving and converting feedback signals from each of the feedback devices; see column 6, lines 26-32, "Thereafter, command data is translated into servo commands for the individual servos 20, 21, and 22, in intrinsic servo signal form. Feedback signals in the intrinsic servo format are likewise returned to the processor 12,

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pre-processed for conversion into the processor base language and utilized in further computations."

With respect to claim 3, applicant contends that Hyatt's processor 12 does not read feedback signals in a cyclic manner. However, as detailed above with reference to column 6, lines 26-32, this is exactly the function performed by processor 12.

With respect to claim 18, applicant contends that Hyatt does not disclose the limitation of "data representative of geometric shapes to be formed in a material comprises a sequence of operations which define the geometric shape." However, Hyatt discloses in column 5, lines 52-57, "The data processor concurrently operates under program control to perform the other aspects of the tack, including carrying out complex computations for tool path control, generating servo commands for each of the controlled axes, sequencing through the program."

Applicant argues with respect to claim 19, that Hyatt's system does not disclose either a user interface or a memory coupled to a single active processor. However, Hyatt clearly discloses in figure 1, a user interface (processor dependent control panel) 14 for communicating with the single active processor 12. Further in figure 1, a core memory 30 is shown for storing the geometric data that will be later processed by processor 12.


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For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

TB 

December 6, 1994


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